

10/14/98

US 503 U.S. PTO

Please type a plus sign (+) inside this box - ☐**UTILITY
PATENT APPLICATION
TRANSMITTAL**(Only for new nonprovisional applications
under 37 CFR 1.53(b))

Attorney Docket No.

2914.IUS

First Inventor or Application Identifier

James E. Green;
Darwin A. Clampitt

Title

HONEYCOMB CAPACITOR AND METHOD OF
FABRICATION

Express Mail Label No.

EJ314420730US

US 503 U.S. PTO
09/172553

10/14/98

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

- 1.
- ☒
- Fee Transmittal Form
-
- (Submit an original, and a duplicate for fee processing)

- 2.
- ☒
- Specification Total Pages
-

(preferred arrangement set forth below)

- Descriptive title of the invention
- Cross References to related Applications
- Statement Regarding Fed Sponsored R&D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

- 3.
- ☒
- Drawing(s) (35 USC 113) Total Sheets
-

4. Oath or Declaration Total Pages
-

a. ☐ Newly executed (original or copy)b. ☒ Copy from a prior application (37
CFR 1.63(d))(For continuation/divisional with Box 17 completed)
(Note Box 5 below)

- i.
- ☐
- DELETION OF INVENTOR(S)**

Signed statement attached deleting
inventor(s) named in the prior
application, see 37 CFR 1.63(d)(2) and
1.33(b).

- 5.
- ☒
- Incorporation By Reference (useable if Box 4b is checked)

The entire disclosure of the prior application, from which a
copy of the oath or declaration is supplied under Box 4b, is
considered as being part of the disclosure of the accompanying
application and is hereby incorporated by reference therein.

- 6.
- ☐
- Microfiche Computer Program (Appendix)

- 7.
- ☐
- Nucleotide and/or Amino Acid Sequence Submission
-
- (if applicable, all necessary)

a. ☐ Computer Readable Copyb. ☐ Paper Copy (identical to computer copy)c. ☐ Statement verifying identity of above copies**ACCOMPANYING APPLICATION PARTS**

- 8.
- ☒
- Assignment Papers (cover sheet & document(s))

- 9.
- ☒
- 37CFR 3.73(b) Statement
- ☒
- Power of Attorney
-
- (when there is an assignee)

- 10.
- ☐
- English Translation Document (if applicable)

- 11.
- ☒
- Information Disclosure
- ☐
- Copies of IDS
-
- Statement (IDS/PTO-1449) Citations

- 12.
- ☒
- Preliminary Amendment

- 13.
- ☒
- Return Receipt Postcard (MPEP 503)

- 14.
- ☐
- Small Entity
- ☐
- Statement filed in prior application,
-
- Statement(s) Status still proper and desired

- 15.
- ☐
- Certified Copy of Priority Document(s)
-
- (If foreign priority is claimed)

- 16.
- ☐
- Other:

*A new statement is required to be entitled to pay small entity fees, except
where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation☒ Divisional☐ Continuation-in-part (CIP)of prior Application No. 08/833,974

Prior application information: Examiner _____ Group/Art Unit: _____

18. CORRESPONDENCE ADDRESS☐ Customer Number or Bar Code Label

below

or ☐ Correspondence address

NAME

Joseph A. Walkowski

TRASK, BRITT & ROSSA

ADDRESS

P.O. Box 2550

CITY

Salt Lake City

STATE

Utah

ZIP CODE

84110

COUNTRY

U.S.A.

TELEPHONE

(801) 532-1922

FAX

(801) 531-9168

Name (Print/Type)

Robert G. Winkle

Registration No. (Attorney/Agent)

37,474

Signature

Date

October 14,
1998

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997.
Small Entity payments must be supported by a small entity statement,
otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT (\$) 954.00

Complete if Known

Application Number	To be assigned
Filing Date	10/14/98
First Named Inventor	James E. Green et al.
Examiner Name	To be assigned
Group / Art Unit	To be assigned
Attorney Docket No.	2914.1US

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number 20-1469
Deposit Account Name Trask, Britt & Rossa

☐ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 ☐ Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. ☒ Payment Enclosed:

☒ Check ☐ Money Order ☐ Other

FEE CALCULATION**1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 790	201 395	Utility filing fee	790
106 330	206 165	Design filing fee	
107 540	207 270	Plant filing fee	
108 790	208 395	Reissue filing fee	
114 150	214 75	Provisional filing fee	
SUBTOTAL (1)			(\$) 790.00

2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
19	-20** = 0	X 22 = 0	
Independent Claims	5	-3** = 2	X 82 = 164
Multiple Dependent			

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
103 22	203 11	Claims in excess of 20	
102 82	202 41	Independent claims in excess of 3	
104 270	204 135	Multiple dependent claim, if not paid	
109 82	209 41	** Reissue independent claims over original patent	
110 22	210 11	** Reissue claims in excess of 20 and over original patent	
SUBTOTAL (2)			(\$) 164.00

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet.	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 400	216 200	Extension for reply within second month	
117 950	217 475	Extension for reply within third month	
118 1,510	218 755	Extension for reply within fourth month	
128 2,060	228 1,030	Extension for reply within fifth month	
119 310	219 155	Notice of Appeal	
120 310	220 155	Filing a brief in support of an appeal	
121 270	221 135	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,320	241 660	Petition to revive - unintentional	
142 1,320	242 660	Utility issue fee (or reissue)	
143 450	243 225	Design issue fee	
144 670	244 335	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 790	246 395	Filing a submission after final rejection (37 CFR 1.129(a))	
149 790	249 395	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify) _____			
Other fee (specify) _____			
SUBTOTAL (3)			(\$)

* Reduced by Basic Filing Fee Paid

SUBMITTED BY

Typed or Printed Name Robert G. Winkle

Signature Robert G. WinkleDate 10/14/98**Complete (if applicable)**Reg. Number 37,474

Deposit Account User ID _____

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Green et al.

Serial No.: To be assigned

Filed: October 14, 1998

For: HONEYCOMB CAPACITOR AND
METHOD OF FABRICATION

Examiner: To be assigned

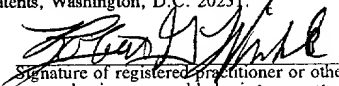
Group Art Unit: To be assigned

Attorney Docket No.: 2914.1US

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

October 14, 1998
Date of Deposit


Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Robert G. Winkle
Typed/printed name of person whose signature is contained above

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the examination of this application on the merits, please amend the above-identified patent application as follows:

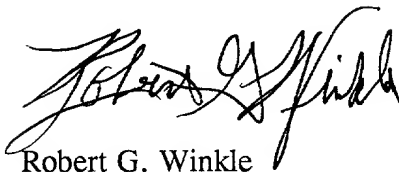
IN THE CLAIMS:

Please cancel claims 1-15 without prejudice.

Entry of the above preliminary amendment is respectfully requested.

This amendment is submitted prior to the issuance of the first Office action.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Robert G. Winkle", written in a cursive style.

Robert G. Winkle
Attorney for Applicants
Registration No. 33,041
P. O. Box 2550
Salt Lake City, UT 84110

RGW/kf
October 14, 1998

N:\2269\2914\pre amd wpd

PATENT
Attorney Docket 2914US(95-0899)

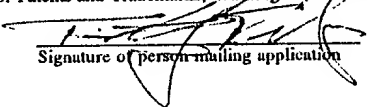
CERTIFICATION UNDER 37 C.F.R. § 1.10

EM548957488US
Express Mail Mailing Label No.

April 11, 1997
Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Timothy Ricks
Typed or printed name
of person mailing application


Signature of person mailing application

APPLICATION FOR LETTERS PATENT

for

HONEYCOMB CAPACITOR AND METHOD OF FABRICATION

Inventors:

James E. Green
Darwin A. Clampitt

Attorney:
Joseph A. Walkowski
Registration No. 28,765
Robert G. Winkle
Registration No. 37,474
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

HONEYCOMB CAPACITOR AND METHOD OF FABRICATION

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to a semiconductor memory device and method of fabricating same. More particularly, the present invention relates to capacitor fabrication techniques applicable to dynamic random access memories ("DRAMs") capable of achieving an improved degree of integration and lower defects within the DRAM.

State of the Art: A widely-utilized DRAM (Dynamic Random Access Memory) manufacturing process utilizes CMOS (Complimentary Metal Oxide Semiconductor) technology to produce DRAM circuits which comprise an array of unit memory cells each including one capacitor and one transistor, such as a field effect transistor ("FET"). In the most common circuit designs, one side of the transistor is connected to external circuit lines called the bit line and the word line, and the other side of the capacitor is connected to a reference voltage that is typically $\frac{1}{2}$ the internal circuit voltage. In such memory cells, an electrical signal charge is stored in a storage node of the capacitor connected to the transistor which charges and discharges circuit lines of the capacitor.

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. The advantage of increased miniaturization of components include: reduced-bulk electronic equipment, improved reliability by reducing the number of solder or plug connections, lower assembly and packaging costs, and improved circuit performance. In pursuit of increased miniaturization, DRAM chips have been continually redesigned to achieved ever higher degrees of integration which has reduced the size of the DRAM. However, as the dimensions of the DRAM are reduced, the occupation area of each unit memory cell of the DRAM must be reduced. This reduction in occupied area necessarily results in a reduction of the dimensions of the

capacitor, which in turn, makes it difficult to ensure required storage capacitance for transmitting a desired signal without malfunction. However, the ability to densely pack the unit memory cells while maintaining required capacitance levels is a crucial requirement of semiconductor manufacturing technologies if future generations of DRAM devices are to be successfully manufactured.

In order to minimize such a decrease in storage capacitance caused by the reduced occupied area of the capacitor, the capacitor should have a relatively large surface area within the limited region defined on a semiconductor substrate. The drive to produce smaller DRAM circuits has given rise to a great deal of capacitor development. However, for reasons of available capacitance, reliability, and ease of fabrication, most capacitors are stacked capacitors in which the capacitor covers nearly the entire area of a cell and in which vertical portions of the capacitor contribute significantly to the total charge storage capacity. In such designs, the side of the capacitor connected to the transistor is generally called the "storage node" or "storage poly" since the material out of which it is formed is doped polysilicon, while the polysilicon layer defining the side of the capacitor connected to the reference voltage mentioned above is called the "cell poly."

An article by J. H. Ahn et al., entitled "Micro Villus Patterning (MVP) Technology for 256 Mb DRAM Stack Cell," 1992 IEEE, 1992 Symposium on VLSI Technology Digest of Technical Papers, pp. 12-13, hereby incorporated herein by reference, discusses the use of MVP (Micro Villus Patterning) technology for forming a high surface area capacitor. FIGs. 25-28 illustrate cross-sectional views of this technique. FIG. 25 shows a memory cell structure comprising a substrate 202 which has been oxidized to form thick field oxide areas 204 with transistor gate members 206 disposed on the surface of the substrate 202. A barrier layer 208 is disposed over the transistor gate members 206, substrate 202, and field oxide areas 204, and a silicon nitride layer 210 is disposed over the barrier layer 208. A storage poly 212 is disposed on the silicon nitride layer 210 and extends through the silicon nitride layer 210 and the

barrier layer 208 and between two transistor gate members 206 to contact the substrate 202. A layer of silicon dioxide 214 is disposed over the storage poly 212.

As shown in FIG. 26, an HSG (HemiSpherical-Grain) polysilicon layer 216 is grown on the exposed surfaces of the silicon nitride layer 210, the storage poly 212, and the silicon dioxide layer 214. The structure is then etched using the HSG polysilicon layer 216 as a mask which results in very thin, closely spaced micro villus bars or pins 218, as shown in FIG. 27. The silicon dioxide layer 214 and the silicon nitride layer 210 are then stripped to form the structure shown in FIG. 28. A finalized capacitor would be formed by further processing steps including depositing a dielectric layer on the etched storage poly and depositing a cell poly on the dielectric layer.

Although the MVP technique greatly increases the surface area of the storage poly, a drawback of using the MVP technique is that it can result in splintering problems (or slivers) in the storage node cell poly. As illustrated in FIG. 29, the micro villus bars/pins 218, formed in the method shown in FIGs. 25-28, are thin and fragile such that they are susceptible to splintering that may result in one or more of the micro villus bars/pins (such as pin 220) falling over and shorting to an adjacent storage poly 222, which would render the adjacent storage cells shorted and unusable.

In a 64M DRAM for example, even if there were only one out of 100,000 cells that had a failure due to a splintered macro villus bar/pin shorting with an adjacent storage cell, it would result in 640 failures or shorts in the DRAM. Generally, there are a limited number of redundant memory cells (usually less than 640 in a 64M DRAM) within a DRAM which are available for use in place of the shorted memory cell. Thus, if the number of failures exceeds the number of redundant memory cells within the DRAM, the DRAM would have to be scrapped.

Therefore, it would be desirable to increase storage cell capacitance by using a technology such as MVP while eliminating polysilicon storage node splintering problems.

SUMMARY OF THE INVENTION

The present invention relates to a method of forming a high surface area capacitor, generally used in DRAMs. The present invention takes an opposite approach from the prior art in forming capacitors. Rather than forming bars or pins to increase the surface area, the present inventions forms the opposite by etching holes or voids into the storage poly to form a honeycomb or webbed structure. Such a honeycomb/webbed structure forms a high surface area capacitor without bars or pins which could splinter and short out an adjacent storage cells, as discussed above.

Numerous methods could be employed to achieve the honeycomb structure of the present invention. One such method is a reverse MVP technique wherein an HSG polysilicon layer is grown on the surface of the storage poly and a mask layer is deposited over the HSG polysilicon layer. An upper portion of the mask layer is then removed forming micro openings to expose the upper most portions of the HSG polysilicon layer. The exposed HSG polysilicon layer portions are then etched, which translates the pattern of the exposed HSG polysilicon layer portions (which is generally the reverse pattern of the bars or pins which would be formed by the prior art method) into the storage poly. The capacitor is completed by depositing a dielectric material layer over the storage poly layer and depositing a cell poly layer over the dielectric material layer.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGs. 1-10 are side cross-sectional views of a method of forming a memory cell capacitor according to the present invention;

FIGs. 11-21 are side cross-sectional views of an alternate technique of forming a memory cell capacitor according to the present invention;

FIG. 22 is an illustration of a scanning electron micrograph of an oblique view of a storage poly after etching in the formation of a capacitor according to the present invention;

FIG. 23 is an illustration of a scanning electron micrograph of a side cross-sectional view of a storage poly after etching in the formation of a capacitor according to the present invention;

FIG. 24 illustrates an oblique, cross-sectional view of FIG. 21;

FIGs. 25-28 are side cross-sectional views of a prior art MVP technique of forming a capacitor by an MVP technique; and

FIG. 29 is a side cross-sectional view of a prior art capacitor formed by a MVP technique which illustrates the problem of storage node splintering.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGs. 1-10 illustrate a technique according to the present invention for forming a capacitor for a memory cell. It should be understood that the figures presented in conjunction with this description (with the exception of FIGs. 22 and 23) are not meant to be actual cross-sectional views of any particular portion of an actual semiconducting device, but are merely idealized representations which are employed to more clearly and fully depict the process of the invention than would otherwise be possible. FIG. 1 illustrates an intermediate structure 100 in the production of a memory cell. This intermediate structure 100 comprises a semiconductor substrate 102, such as a lightly doped P-type crystal silicon substrate, which has been oxidized to form thick field oxide areas 104 and exposed to implantation processes to form drain regions 106 and source regions 107. Transistor gate members 108 are formed on the surface of the semiconductor substrate 102, including the gate members 108 residing on a substrate active area 118 spanned between the drain regions 106 and the source regions 107.

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The transistor gate members 108 each comprise a lower buffer layer 110, preferably silicon dioxide, separating a gate conducting layer or wordline 112 of the transistor gate member 108 from the semiconductor substrate 102. Transistor insulating spacer members 114, preferably silicon dioxide, are formed on either side of each transistor gate member 108 and a cap insulator 116, also preferably silicon dioxide, is formed on the top of each transistor gate member 108. A barrier layer 119, preferably silicon dioxide, is disposed over the semiconductor substrate 102, the thick field oxide areas 104, and the transistor gate members 108, and etched to expose the drain regions 106 on the semiconductor substrate 102. A storage poly 120, such as a polysilicon material, is deposited over the transistor gate members 108, the semiconductor substrate 102, and the thick field oxide areas 104.

An HSG (HemiSpherical-Grain) polysilicon layer 122 is grown on the surface of the storage poly 120, as shown in FIG. 2 (which is an enlarged view of the surface of the storage poly 120). Preferably, the HSG polysilicon layer 122 is grown by applying a layer of amorphous silicon over the storage poly 120. A polysilicon seed crystal layer is applied at a temperature of at least 500°C, preferably between about 550 and 600°C, and a pressure between about 10^{-7} and 10^{-2} Torr. The polysilicon seed crystal layer is then annealed at a temperature of at least 500°C, preferably between about 550 and 700°C, and a pressure between about 10^{-7} and 10^{-2} Torr. The annealing causes the amorphous silicon to nucleate into a polysilicon material around the polysilicon seed crystal to form the HSG polysilicon layer 122. The grain size of the HSG polysilicon should be at least 350Å, preferably between about 700 and 1000Å. The HSG polysilicon formation process can be accomplished in batch (multi-wafer) or single wafer equipment.

A mask layer 124, preferably silicon dioxide with a thickness of about 350 angstroms, is deposited over the HSG polysilicon layer 122, as shown in FIG. 3. An upper portion of the mask layer 124 is then removed, preferably facet etched (dry etching, sputter etching, and planarization may also be used), to form micro openings

to expose the upper-most portions 126 of the HSG polysilicon layer 122, as shown in FIG. 4. Preferably, about 50 to 75% of the HSG polysilicon layer 122 will be exposed. As shown in FIG. 5, a photo-resist material 128 is then deposited to pattern a desired position of the memory cell capacitor (the HSG polysilicon layer 122 and the mask layer 124 are shown as a single layer 130).

As shown in FIG. 6, a portion of the single layer 130 and a portion of the storage poly 120 are etched to expose a portion of the barrier layer 119 over the source region 107, the thick field oxide 104, and a portion of the gate members 108. The photo-resist material 128 is then removed.

The exposed upper-most HSG polysilicon layer portions 126 are then etched with a dry anisotropic etch, with an etchant which is highly selective to the mask layer 124, preferably selective at a ratio of about 70:1 or higher, as shown in progress in FIG. 8. A preferred selective etch chemistry would contain chlorine gas as the primary etchant with passivation for the barrier layer 119 (silicon dioxide) is hydrogen bromide gas (i.e., the hydrogen bromide prevents the etching of the silicon dioxide barrier layer 119 which, in turn, prevents the source region 107 from being etched). Selective etching is the use of particular etchants which etch only a particular material or materials while being substantially inert to other materials.

The etching translates the pattern of the exposed upper-most HSG polysilicon layer portions 126 into the storage poly 120. Any remaining mask layer material 124 is then removed, preferably by a wet or in situ etch. The etching of the storage poly 120 results in an etched structure 132 having convoluted openings 134, shown with the convoluted openings 134 greatly exaggerated in FIG. 9. Capacitors 136 are completed by depositing a dielectric material layer 138 over the etched structure 132 and depositing a cell poly layer 140 over the dielectric material layer 138, such as shown in FIG. 10.

It is, of course, understood that the present invention is not limited to any single technique forming the memory cell capacitor. For example, FIGs. 11-21 illustrate an

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alternate memory cell capacitor formation technique. Elements common to both FIGs. 1-10 and FIGs. 11-21 retain the same numeric designation. FIG. 11 shows a first barrier layer 142, preferably tetraethyl orthosilicate - TEOS, disposed over the semiconductor substrate 102, the thick field oxide areas 104, and the transistor gate members 108. The transistor gate members 108 each comprise a lower buffer layer 109, preferably silicon dioxide or silicon nitride, separating the gate conducting layer or wordline 112 of the transistor gate member 108 from the semiconductor substrate 102. Transistor insulating spacer members 113, made of silicon nitride, are formed on either side of each transistor gate member 108 and a cap insulator 115, also made of silicon nitride, is formed on the top of each transistor gate member 108. Preferably, the gate members 108 residing on the thick field oxide areas 104 abut the active area 118 which will protect the thick field oxide areas 104 during subsequent etching. A second barrier layer 144 (preferably made of borophosphosilicate glass - BPSG, phosphosilicate glass - PSG, or the like) is deposited over the first barrier layer 142, as shown in FIG. 12.

It is, of course, understood that a single barrier layer could be employed. However, a typical barrier configuration is a layer of TEOS over the transistor gate members 108 and the substrate 102 followed by a BPSG layer over the TEOS layer. The TEOS layer is applied to prevent dopant migration. The BPSG layer contains boron and phosphorus which can migrate into the source and drain regions formed on the substrate during inherent device fabrication heating steps. This migration of boron and phosphorus can change the dopant concentrations in the source and drain regions which can adversely affect the performance of the memory cell.

As shown in FIG. 13, a resist material 146 is patterned on the second barrier layer 144, such that predetermined areas of the memory cell capacitor formation will be etched. The second barrier layer 144 and the first barrier layer 142 are etched to exposed a portion of the semiconductor substrate 102, as shown in FIG. 14. The transistor insulating spacer members 113 and the cap insulator 115 each being made of

silicon nitride resists the etchant and thus prevents shorting between the word line 112 and the capacitor to be formed. The resist material 146 is then removed, as shown in FIG. 15, and a layer of amorphous silicon 148, which upon subsequent annealing will become polysilicon, is then applied over second barrier layer 144 to make contact with the semiconductor substrate 102, as shown in FIG. 16. The amorphous silicon layer 148 is then planarized down to the second barrier layer 144 to form silicon plugs 150, as shown in FIG 17. The planarization is preferably performed using a mechanical abrasion, such as a chemical mechanical planarization (CMP) process.

An HSG polysilicon layer 122 is selectively grown on the surface of the silicon plugs 150, as shown in FIG. 18. The selectively growth the HSG polysilicon layer 122 is preferably achieved by applying a polysilicon seed crystal layer over the second barrier layer 144 and the silicon plugs 150. The polysilicon seed crystal layer is applied at a temperature of at least 500°C, preferably between about 550 and 600°C, and a pressure between about 10^{-7} and 10^{-2} Torr. The polysilicon seed crystal layer is then annealed at a temperature of at least 500°C, preferably between about 550 and 700°C, and a pressure between about 10^{-7} and 10^{-2} Torr. The selectivity of growth of the HSG polysilicon layer 122 is due to the difference in incubation times required to seed nucleation sites for the HSG polysilicon layer 122 on the silicon plugs 150 (amorphous silicon) and the second barrier layer 144. The HSG nucleation sites form more quickly on the silicon plugs 150 than on the second barrier layer 144. Thus, the HSG polysilicon growth can be completed on the silicon plugs 150 and the formation halted prior to the formation of HSG polysilicon on the second barrier layer 144.

A mask layer 124 is deposited over the HSG polysilicon layer 122. The upper portion of the mask layer 124 is then removed to expose the upper-most portions 126 of the HSG polysilicon layer 122, as shown in FIG. 20. The exposed HSG polysilicon layer portions 126 are then etched, as previously shown in FIG. 8. The etching of the silicon plugs 150 results in an etched structure 152 having convoluted openings 154, shown with the convoluted openings 154 greatly exaggerated in FIG. 21. The memory

cell capacitors are completed by depositing a dielectric material layer over the etched structure 152 and depositing a cell poly layer over the dielectric material layer, as previously described for FIG. 10.

The method of the present invention results in a unique honeycomb storage poly structure such that the storage poly has a highly webbed structure rather than free standing micro villus bar/pin structures, as discussed above. This webbed structure is essentially a substantially continuous, convoluted maze-like structure defined by a plurality of interconnected wells extending in various directions in the X-Y plane. In other words, the maze-like structure extends in the X, Y, and Z coordinates, rather than essentially only in the Z coordinate in which a free standing micro villus bar/pin structure with limited extent in the X-Y plane would essentially only exist. An exemplary illustration of a typical pattern in the X-Y plane is shown in FIG. 22. FIG. 22 is an illustration of a scanning electron micrograph, top view, of the etched structure 132 or 152 after etching same and after removal of any remaining mask layer material 124. As FIG. 22 illustrates, the etched structure 132, 152 is highly integrated/webbed. Another way to visualize the resulting structure is in terms of canyons and holes between interconnected mesas or ridges defining a convoluted topography.

The integrated/webbed structure of the storage poly 120 in the X and Z coordinate is shown in FIG. 23. FIG. 23 is an illustration of a scanning electron micrograph, side cross-sectional view, of the storage poly. FIG. 24 illustrates an oblique, cross-sectional view of the etched structure 152 of FIG. 21. This maze-like webbed structure is substantially self-buttressing. In other words, the convoluted and webbed shape forms a strong structure which allows the capacitor to withstand forces which would otherwise splinter a micro villus pin/bar capacitor.

* * * * *

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope thereof.

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CLAIMS

What is claimed is:

1. A method of producing a storage poly structure for a semiconductor capacitor, comprising:
- 5 providing a storage poly;
growing a hemispherical-grain polysilicon layer on said storage poly;
applying a mask layer over said hemispherical-grain polysilicon layer;
removing an upper portion of said mask layer to expose elevated portions of said
hemispherical-grain polysilicon layer; and
10 etching through said exposed portions of said hemispherical grain polysilicon layer
portions and into said storage poly.
2. The method of claim 1, further comprising:
depositing a photo-resist material on said storage poly to pattern a desired position of
15 said storage poly structure;
etching said storage poly; and
removing said photo-resist material prior to etching through said hemispherical grain
polysilicon layer exposed portions.
3. The method of claim 1, wherein providing a storage poly comprises:
depositing a buffer layer on a semiconductor substrate;
20 patterning a resist material on said buffer layer wherein open areas in said resist
material are position in desired areas for formation of said storage poly
structure;
25 etching said buffer layer to expose portions of said semiconductor substrate;
removing said resist material;
applying a layer of polysilicon over said barrier layer wherein said polysilicon layer
contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

4. The method of claim 3, wherein planarizing is performed using a mechanical abrasion.

5. The method of claim 4, wherein said mechanical abrasion is a chemical mechanical planarization process.

6. A method of producing a semiconductor capacitor, comprising:
providing storage poly;
growing a hemispherical-grain polysilicon layer on said storage poly;
applying a mask layer over said hemispherical-grain polysilicon layer;
removing an upper portion of said mask layer to expose elevated portions of said
hemispherical-grain polysilicon layer;
etching through said exposed portions of said hemispherical grain polysilicon layer
portions and into said storage poly;
depositing a dielectric material over said etched storage poly; and
depositing a cell poly over said dielectric material.

7. The method of claim 6, further comprising:
depositing a photo-resist material on said storage poly to pattern a desired position of
said storage poly structure;
etching said storage poly; and
removing said photo-resist material prior to etching through said hemispherical grain
polysilicon layer exposed portions.

8. The method of claim 6, wherein providing a storage poly comprises:
depositing a buffer layer on a semiconductor substrate;

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patterning a resist material on said buffer layer wherein open areas in said resist material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

5 removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

10 9. The method of claim 8, wherein planarizing is performed using a mechanical abrasion.

10. The method of claim 9, wherein said mechanical abrasion is a chemical mechanical planarization process.

15 11. A method of producing a semiconductor memory cell, comprising:
providing an intermediate structure comprising a semiconductor substrate including at least one field oxide area and at least one active area containing at least one drain region and at least one source region, at least one transistor gate member residing on said substrate active area spanned between said at least one drain region and said at least one source region, and a storage poly which is in contact with the semiconductor substrate;

growing a hemispherical-grain polysilicon layer on said storage poly;

applying a mask layer over said hemispherical-grain polysilicon layer;

25 removing an upper portion of said mask layer to expose elevated portions of said hemispherical-grain polysilicon layer;

etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly;

depositing a dielectric material over said etched storage poly; and
depositing a cell poly over said dielectric material.

12. The method of claim 11, wherein said storage poly of said intermediate
5 structure is formed by:

applying a storage poly layer over said at least one field oxide area, said at least one
active area, and said at least one transistor gate member;
depositing a photo-resist material on said storage poly to pattern a desired position of
said storage poly structure;
10 etching said storage poly; and
removing said photo-resist material prior to etching through said hemispherical grain
polysilicon layer exposed portions.

13. The method of claim 11, wherein said storage poly of said intermediate
15 structure is formed by:

depositing a buffer layer over said at least one field oxide area, said at least one active
area, and said at least one transistor gate member;
patterning a resist material on said buffer layer wherein open areas in said resist
material are position in desired areas for formation of said storage poly
20 structure;
etching said buffer layer to expose at least a portion of said active area;
removing said resist material;
applying a layer of polysilicon over said barrier layer wherein said polysilicon layer
contacts said semiconductor substrate; and
25 planarizing said polysilicon layer to the barrier layer forming said storage poly.

14. The method of claim 13, wherein planarizing is performed using a
mechanical abrasion.

15. The method of claim 14, wherein said mechanical abrasion is a chemical mechanical planarization process.

5 16. A storage poly structure for a semiconductor capacitor formed by the method comprising:
providing a storage poly;
growing a hemispherical-grain polysilicon layer on said storage poly;
applying a mask layer over said hemispherical-grain polysilicon layer;
removing an upper portion of said mask layer to expose elevated portions of said
10 hemispherical-grain polysilicon layer; and
etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly.

15 17. The storage poly structure of claim 16, further comprising:
depositing a photo-resist material on said storage poly to pattern a desired position of said storage poly structure;
etching said storage poly; and
removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

20 18. The storage poly structure of claim 16, wherein providing a storage poly comprises:
depositing a buffer layer on a semiconductor substrate;
patterning a resist material on said buffer layer wherein open areas in said resist
25 material are position in desired areas for formation of said storage poly structure;
etching said buffer layer to expose portions of said semiconductor substrate;
removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer
contacts said semiconductor substrate; and
planarizing said polysilicon layer to the barrier layer forming said storage poly.

5 19. The storage poly structure of claim 18, wherein planarizing is performed
using a mechanical abrasion.

 20. The storage poly structure of claim 19, wherein said mechanical abrasion
is a chemical mechanical planarization process.

10 21. A semiconductor capacitor produced by the method comprising:
providing storage poly;
growing a hemispherical-grain polysilicon layer on said storage poly;
applying a mask layer over said hemispherical-grain polysilicon layer;
15 removing an upper portion of said mask layer to expose elevated portions of said
hemispherical-grain polysilicon layer;
etching through said exposed portions of said hemispherical grain polysilicon layer
portions and into said storage poly;
depositing a dielectric material over said etched storage poly; and
20 depositing a cell poly over said dielectric material.

 22. The semiconductor capacitor of claim 21, further comprising:
depositing a photo-resist material on said storage poly to pattern a desired position of
said storage poly structure;
25 etching said storage poly; and
removing said photo-resist material prior to etching through said hemispherical grain
polysilicon layer exposed portions.

23. The semiconductor capacitor of claim 21, wherein providing a storage poly comprises:

depositing a buffer layer on a semiconductor substrate;

patterning a resist material on said buffer layer wherein open areas in said resist

5 material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer

10 contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

24. The semiconductor capacitor of claim 23, wherein planarizing is performed using a mechanical abrasion.

15 25. The semiconductor capacitor of claim 24, wherein said mechanical abrasion is a chemical mechanical planarization process.

26. A semiconductor memory cell produced by a method comprising:
20 providing an intermediate structure comprising a semiconductor substrate including at least one field oxide area and at least one active area containing at least one drain region and at least one source region, at least one transistor gate member residing on said substrate active area spanned between said at least one drain region and said at least one source region, and a storage poly which is in
25 contact with the semiconductor substrate;

growing a hemispherical-grain polysilicon layer on said storage poly;

applying a mask layer over said hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of said
hemispherical-grain polysilicon layer;
etching through said exposed portions of said hemispherical grain polysilicon layer
portions and into said storage poly;
5 depositing a dielectric material over said etched storage poly; and
depositing a cell poly over said dielectric material.

27. The semiconductor memory cell of claim 26, wherein said storage poly
of said intermediate structure is formed by:

10 applying a storage poly layer over said at least one field oxide area, said at least one
active area, and said at least one transistor gate member;
depositing a photo-resist material on said storage poly to pattern a desired position of
said storage poly structure;
etching said storage poly; and
15 removing said photo-resist material prior to etching through said hemispherical grain
polysilicon layer exposed portions.

28. The semiconductor memory cell of claim 26, wherein said storage poly
of said intermediate structure is formed by:

20 depositing a buffer layer over said at least one field oxide area, said at least one active
area, and said at least one transistor gate member;
patterning a resist material on said buffer layer wherein open areas in said resist
material are position in desired areas for formation of said storage poly
structure;
25 etching said buffer layer to expose at least a portion of said active area;
removing said resist material;
applying a layer of polysilicon over said barrier layer wherein said polysilicon layer
contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

29. The semiconductor memory cell of claim 28, wherein planarizing is performed using a mechanical abrasion.

5

30. The semiconductor memory cell of claim 29, wherein said mechanical abrasion is a chemical mechanical planarization process.

10

31. A semiconductor capacitor storage poly comprising a plurality of contiguous mesas forming a maze-like structure.

32. The storage poly of claim 31, wherein said mesas extend in the X, Y and Z coordinates.

15

33. A semiconductor capacitor storage poly comprising a plurality of contiguous webs forming a maze-like structure.

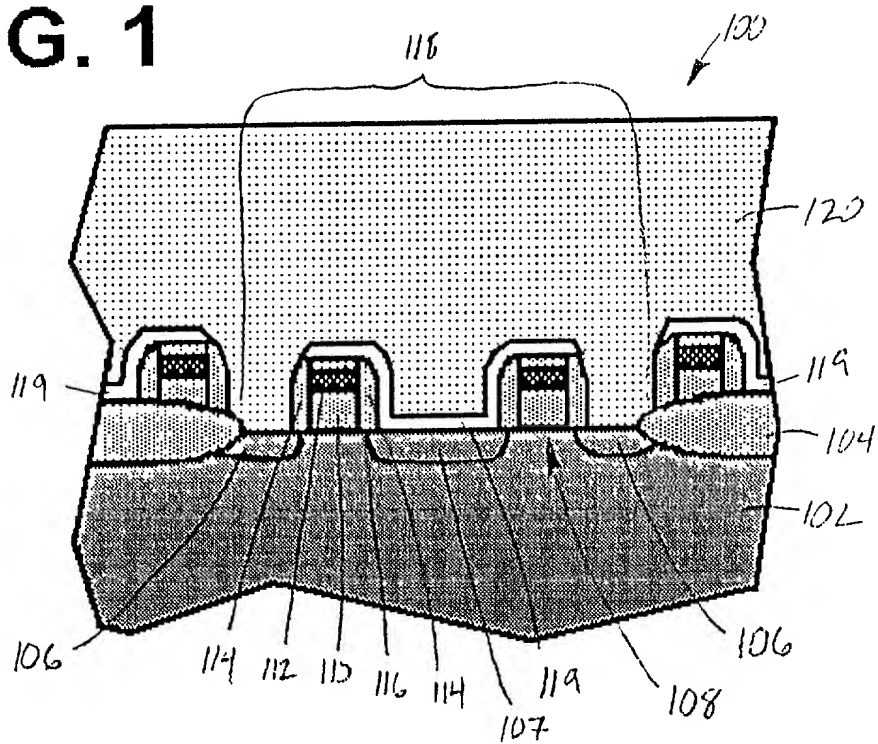
34. The storage poly of claim 31, wherein said webs extend in the X, Y and Z coordinates.

ABSTRACT

A honeycomb/webbed, high surface area capacitor formed by etching a storage poly using an etch mask having a plurality of micro vias. The etch mask is preferably formed by applying an HSG polysilicon layer on a surface of the storage poly with a mask layer being deposited over the HSG polysilicon layer. An upper portion of the mask layer is removed to expose the upper most portions of the HSG polysilicon layer and the exposed HSG polysilicon layer portions are then etched which translates the pattern of the exposed HSG polysilicon layer portions into the storage poly. The capacitor is completed by depositing a dielectric material layer over the storage poly layer and depositing a cell poly layer over the dielectric material layer.

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FIG. 1



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FIG. 2

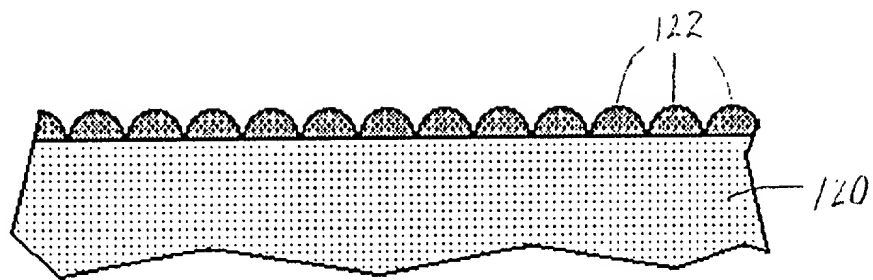


FIG. 3

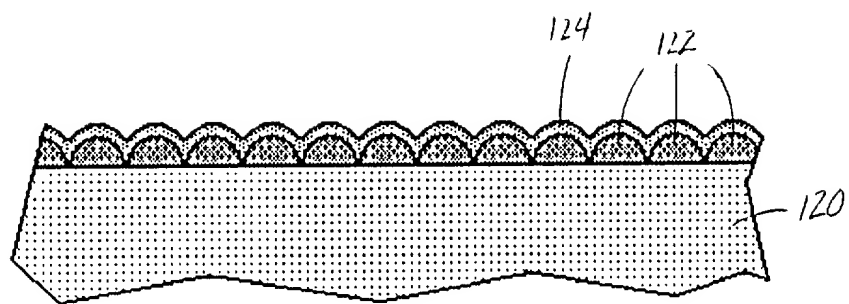


FIG. 4

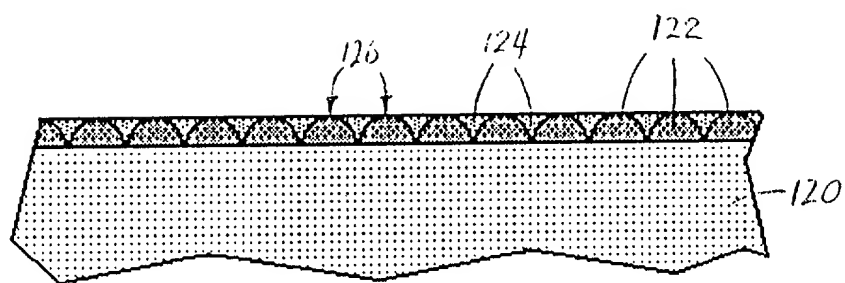


FIG. 5

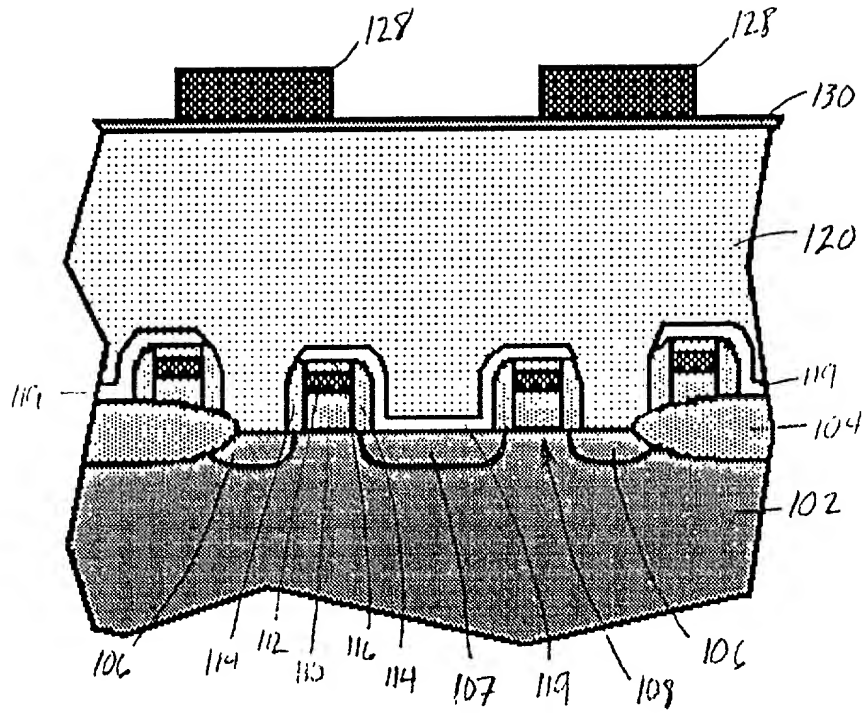


FIG. 6

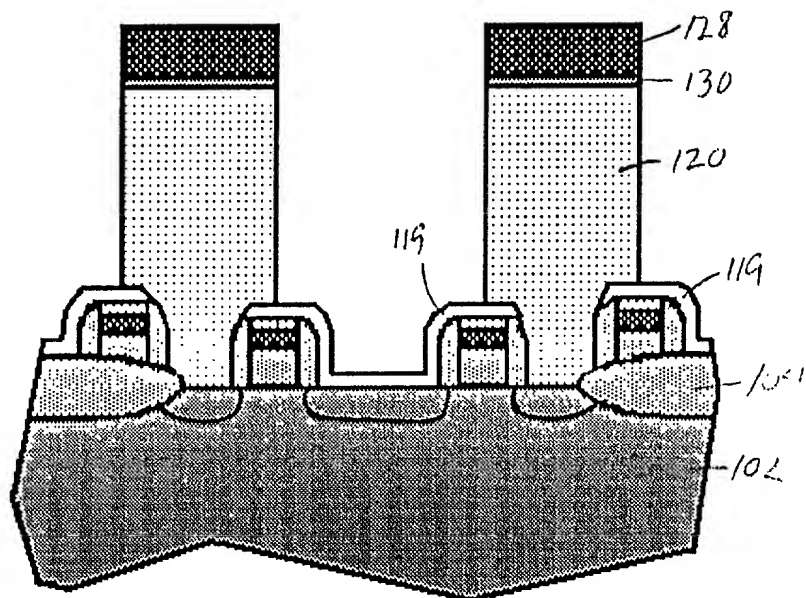
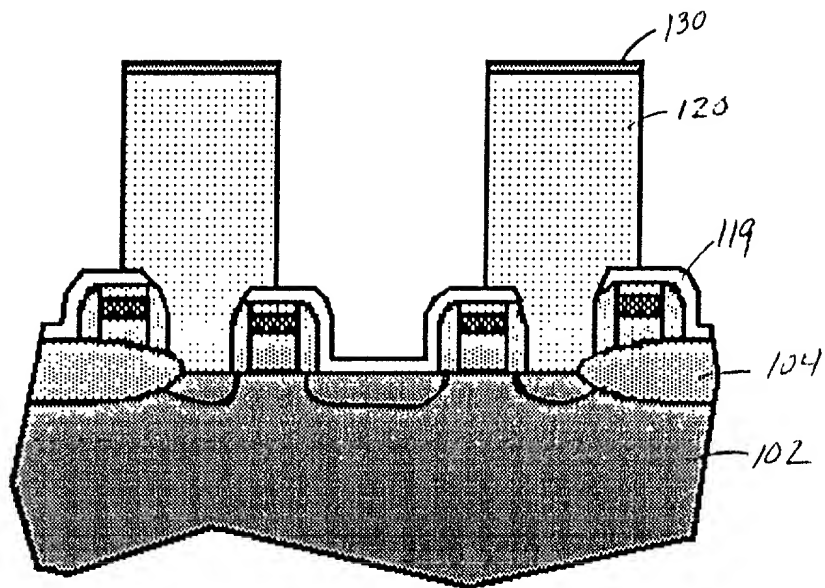


FIG. 7



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FIG. 8

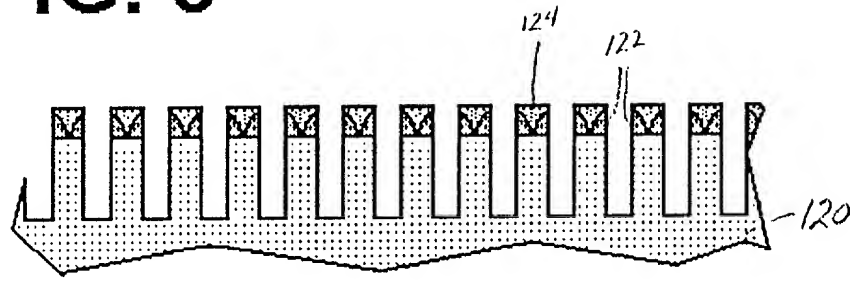


FIG. 9

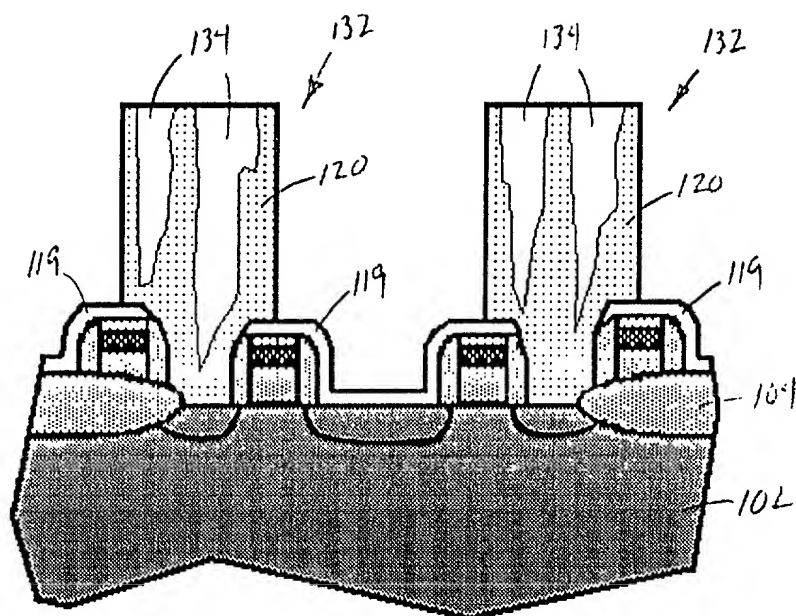
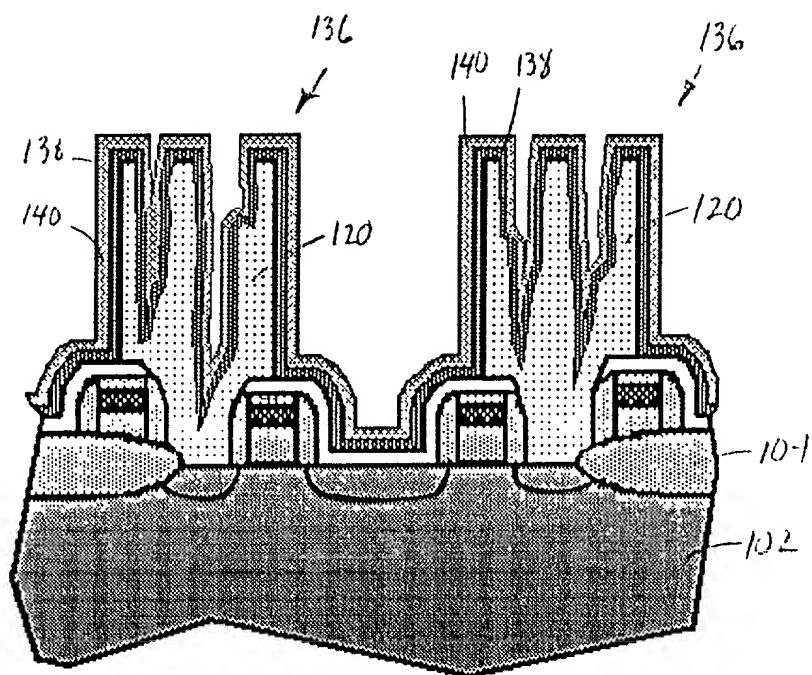


FIG. 10



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FIG. 12

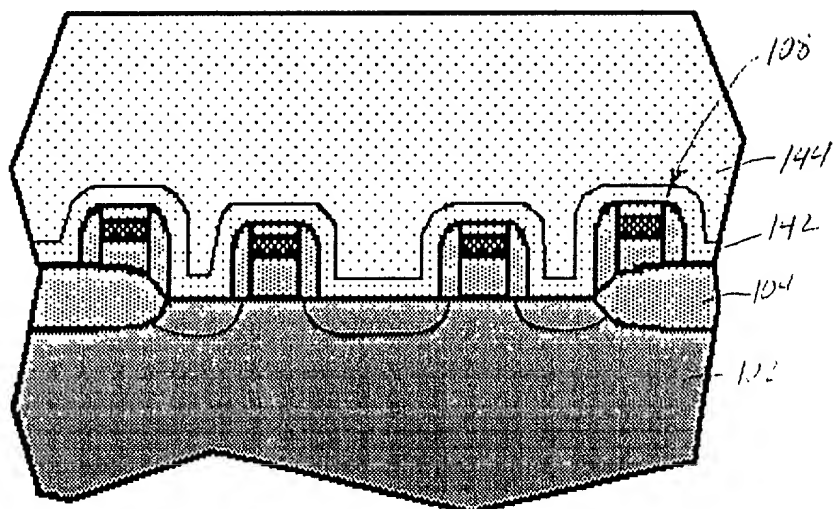


FIG. 13

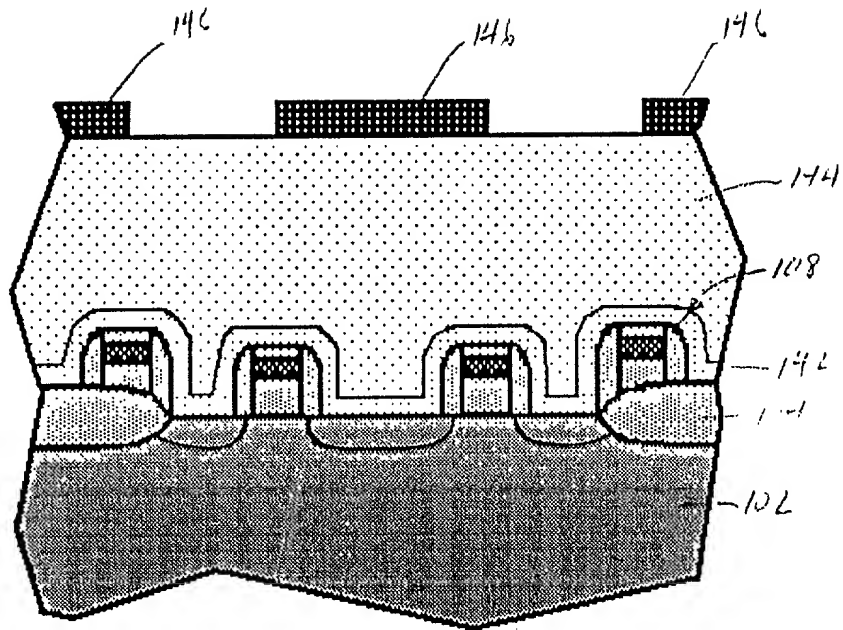


FIG. 14

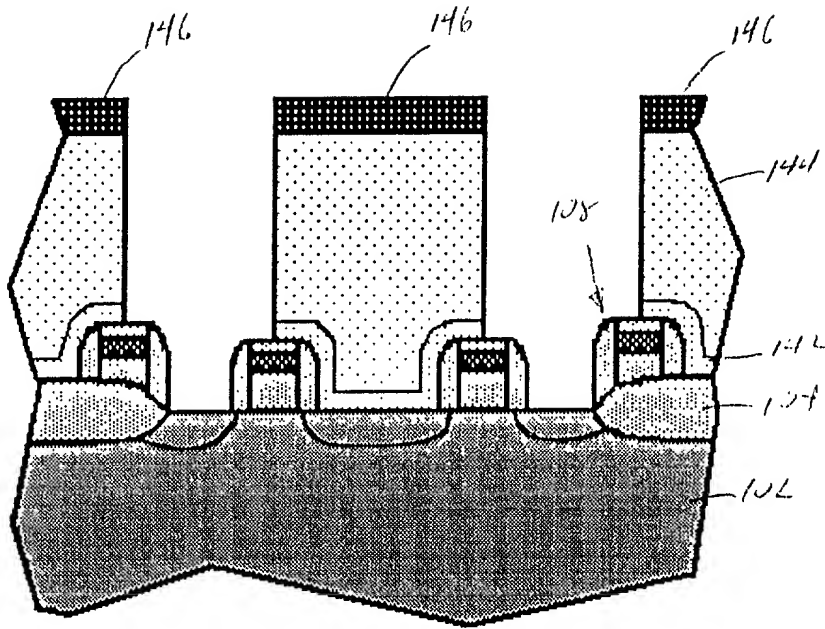


FIG. 15

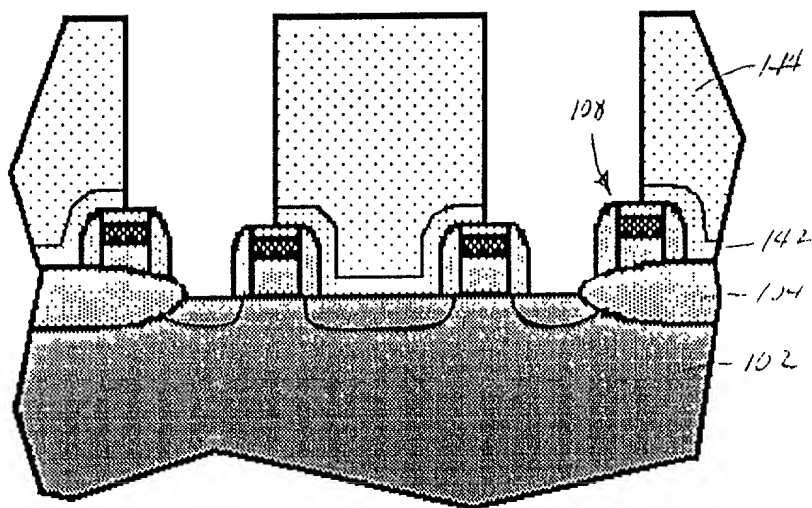


FIG. 16

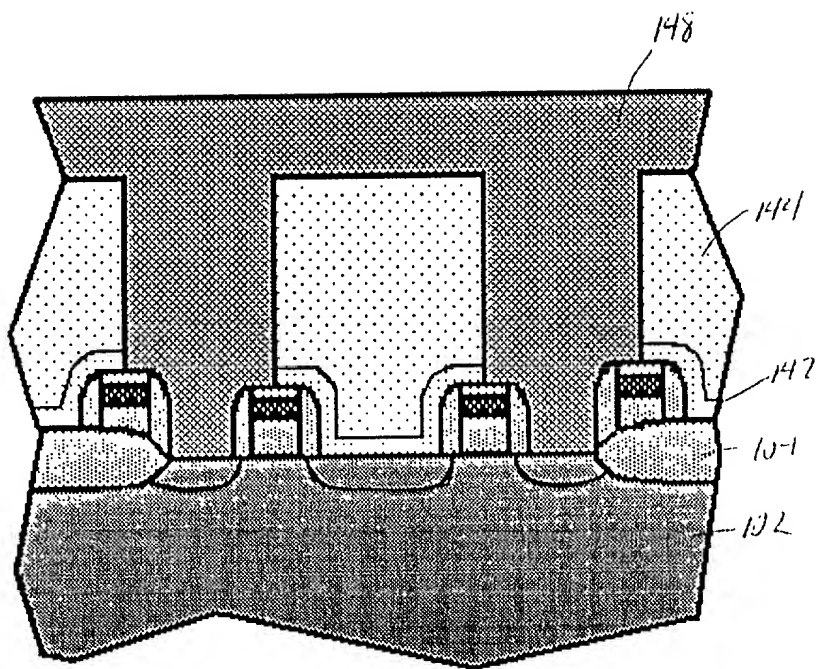


FIG. 17

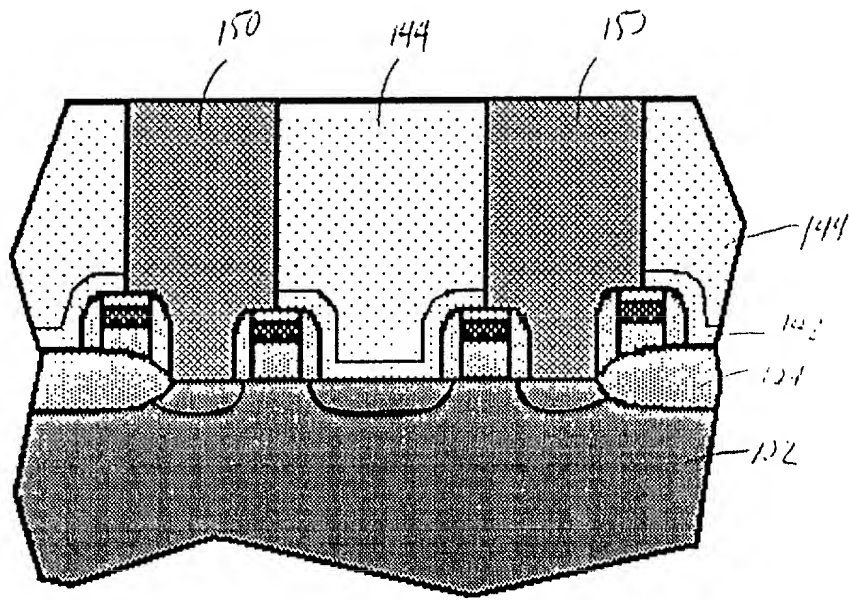
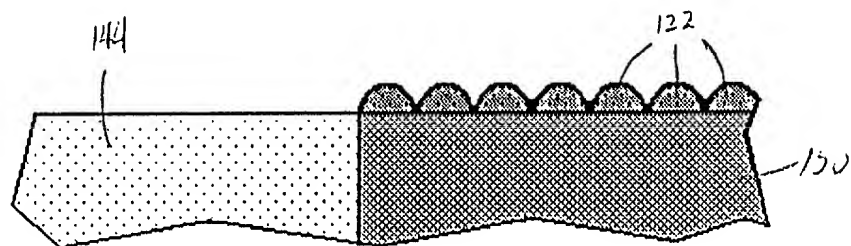
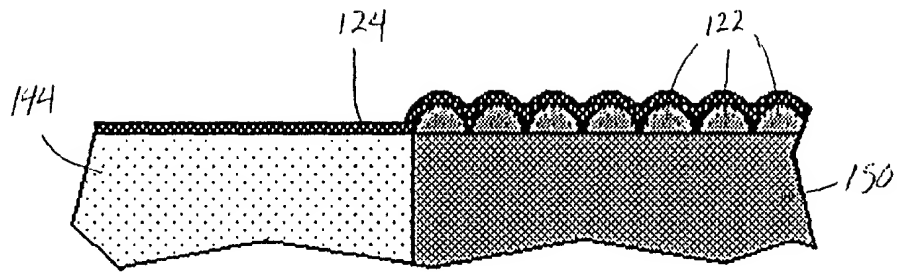


FIG. 18



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FIG. 19



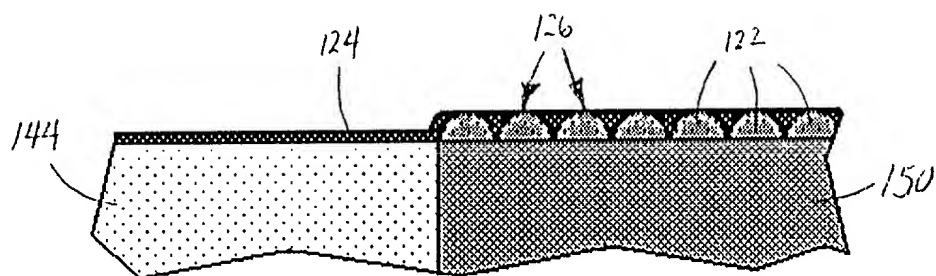
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FIG. 21

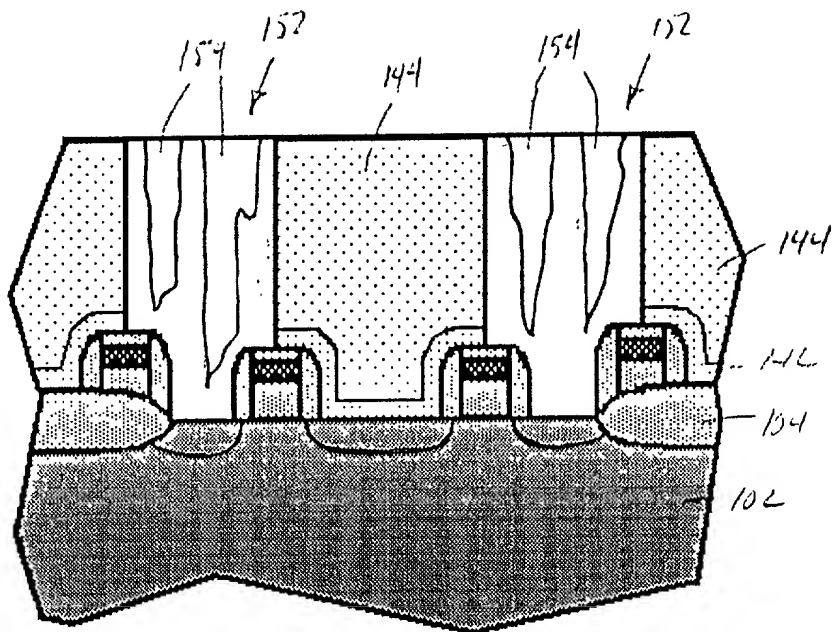
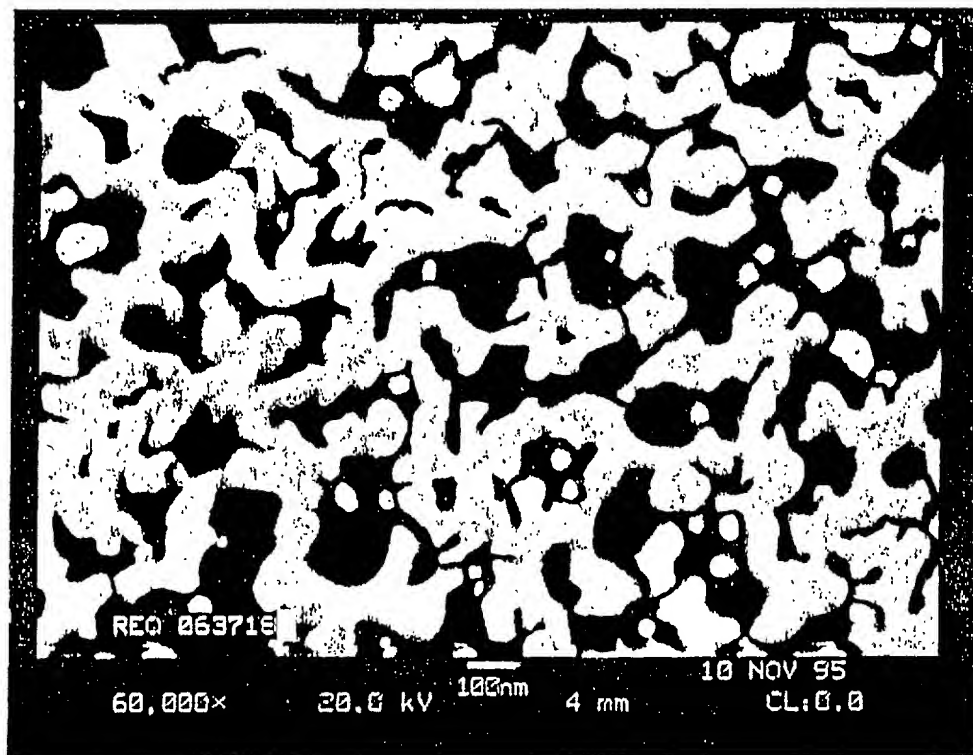


FIG. 22



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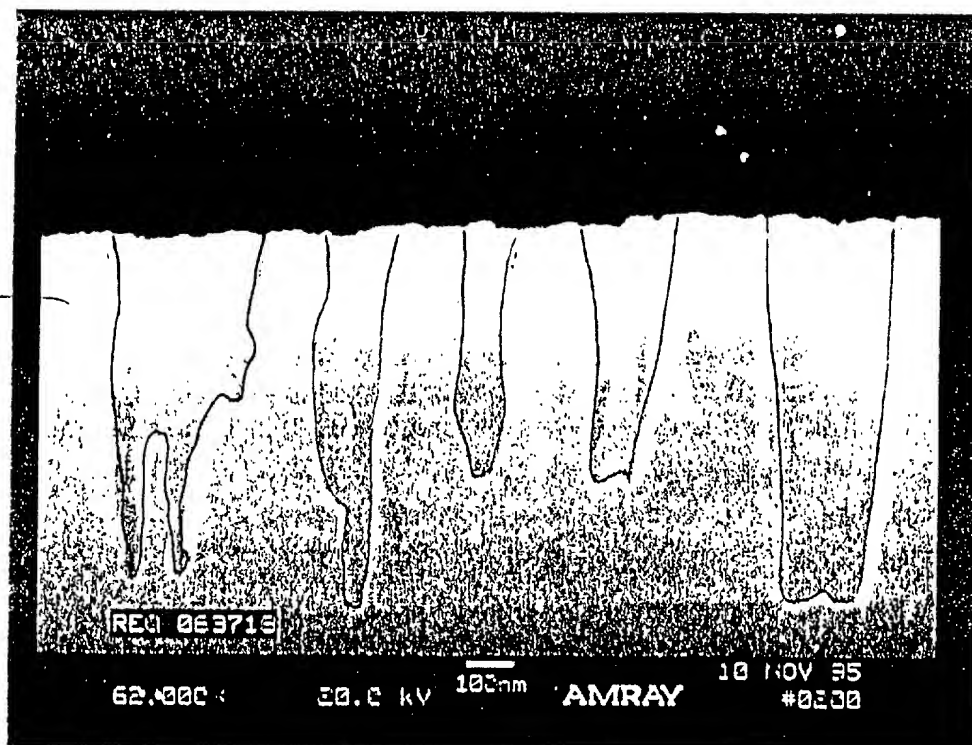
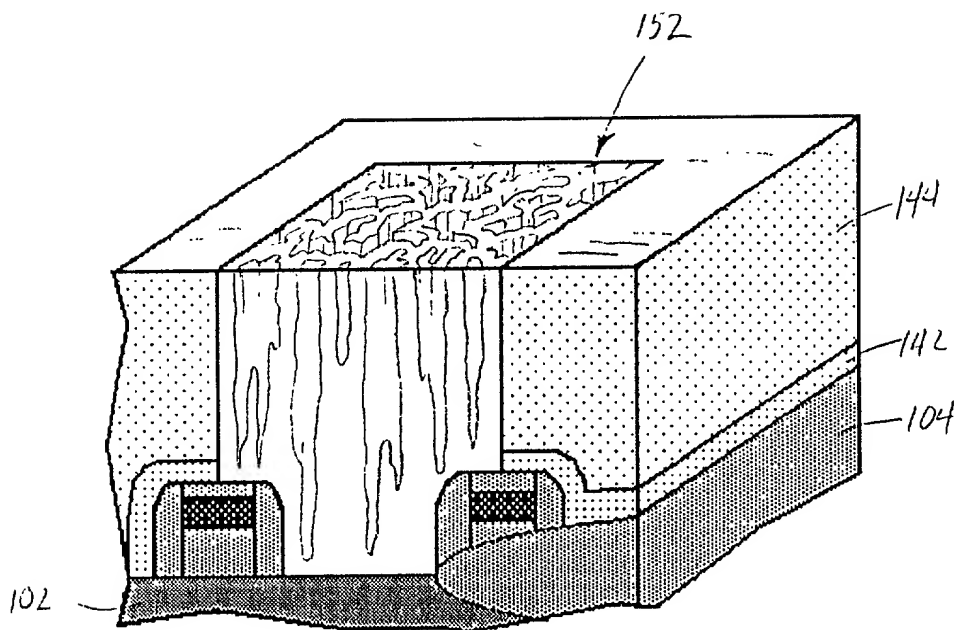


FIG. 24



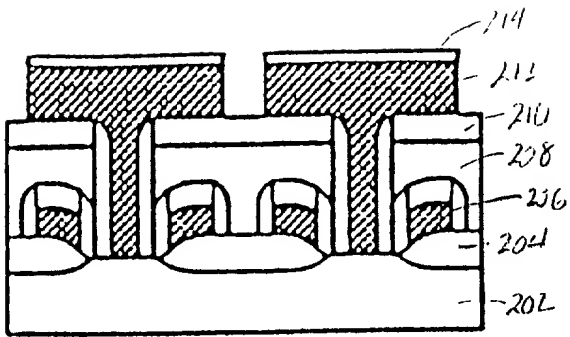


FIG. 25

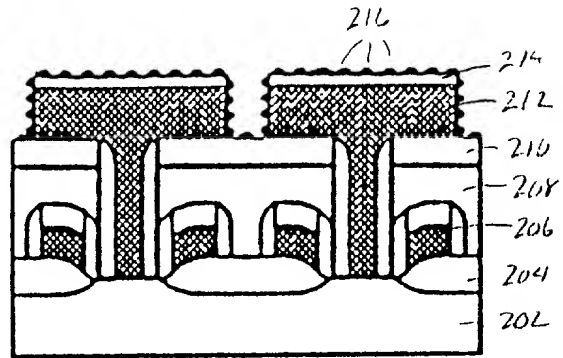


FIG. 26

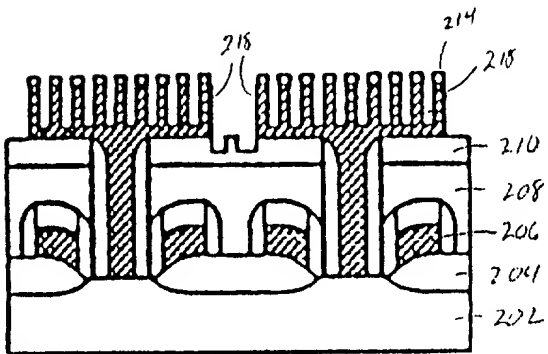


FIG. 27

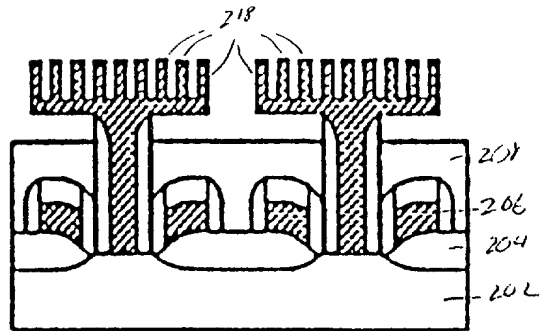
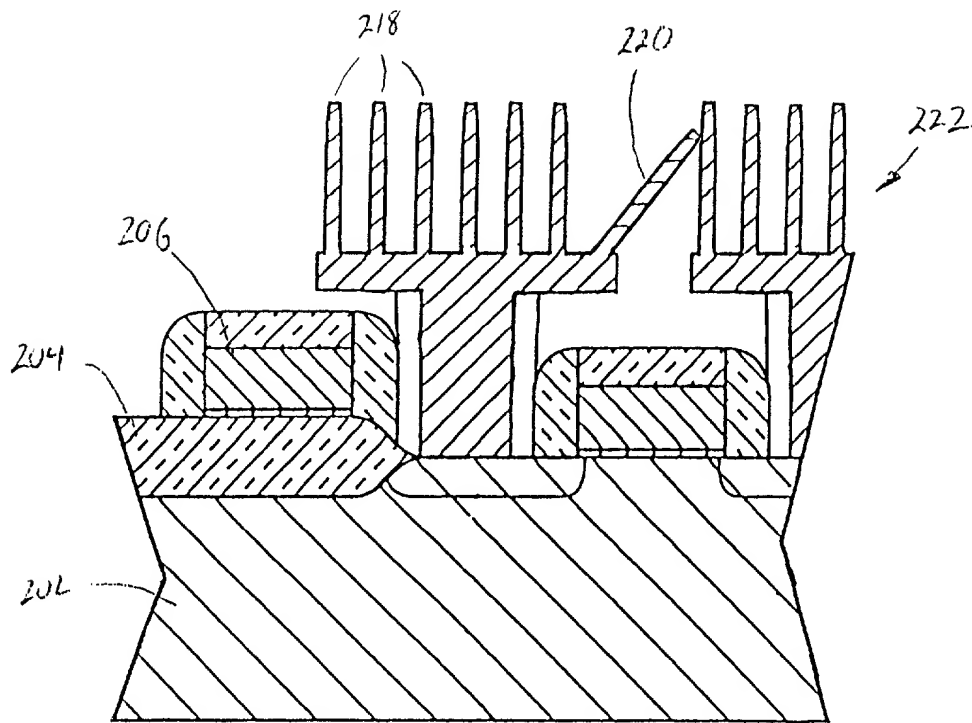


FIG. 28

FIG. 29



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DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **HONEYCOMB CAPACITOR AND METHOD OF FABRICATION**, the specification of which (check one):

☒ is attached hereto.

☐ was filed on _____ as United States application serial no. _____ and was amended on _____.

☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
_____	_____	_____	_____	_____
(number)	(country)	(day/month/year filed)	Yes	No
_____	_____	_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
_____	_____	_____
(application serial no.)	(filing date)	(status - pending, patented or abandoned)
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
_____	_____
(provisional application no.)	(filing date)
_____	_____
(provisional application no.)	(filing date)
_____	_____

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012
Laurence B. Bond, Reg. No. 30,549
Allen C. Turner, Reg. No. 33,041
Robert G. Winkle, Reg. No. 37,474
Edgar R. Cataxinos, Reg. No. 39,931

William S. Britt, Reg. No. 20,969
Joseph A. Walkowski, Reg. No. 28,765
Kent S. Burningham, Reg. No. 30,453
Patrick McBride, Reg. No. 39,295
Michael L. Lynch, Reg. No. 30,871

Thomas J. Rossa, Reg. No. 26,799
James R. Duzan, Reg. No. 28,393
Julie K. Morriss, Reg. No. 33,263
Frank W. Compagni, Reg. No. P-40,567
Lia M. Pappas, Reg. No. 34,095

Address all correspondence to:

Joseph A. Walkowski, telephone no. (801) 532-1922.
TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: James E. Green

Inventor's signature

Residence: Caldwell, Idaho 83605

Citizenship: United States of America

Post Office Address: 1415 Nth 4th St., Caldwell, Idaho 83605

Date

4-09-97

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention title:

Inventor name(s) appearing on first declaration page:

☒ Additional original, first and joint inventor(s):

Full name of second joint inventor: Darwin A. Clampitt

Inventor's signature

Residence: Boise, Idaho 83706

Citizenship: United States of America

Post Office Address: 3712 Clegg Street, Boise, Idaho 83706

Date

04-09-97

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